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MANUFACTURING METHOD FOR PRINTED WIRING SUBSTRATE FOR SEMICONDUCTOR MOUNTING

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[There are no amendments to this patent.]

Claims

1. Manufacturing method for printed wiring substrate for semiconductor mounting is composed of processes (a)-(e) below.

(a) a process in which multiple conductor pattern groups that have through-holes are formed, which are arranged longitudinally and laterally on printed wiring substrate sheet (1) that is composed of an organic resin material;

(b) a process where part of the through-holes (2) on the external outline of the finished product and part of the substrate (3) are cut away in each of the conductor pattern groups on the aforementioned printed wiring substrate sheet to form grooves around the through-holes, and bridge parts (4) are formed between said grooves;

(c) a process in which the grooves corresponding to the groups of finished products on the aforementioned printed wiring substrate and through-holes around the parts where the semiconductors are mounted are furnished in another stacked substrate sheet that is composed of an organic resin material, and bridge parts are formed and arranged;

(d) a process in which the stacked substrate sheet produced in aforementioned process (c) is stuck with an adhesive layer onto the surface of the printed wiring substrate sheet produced in aforementioned processes (a) and (b);

(e) a process in which the bridge parts of the printed wiring substrate sheets produced in aforementioned process (d) are cut and separated into pieces to form multiple groups of finished products.

2. Manufacturing method for printed wiring substrate for semiconductor mounting described in Claim 1, characterized in that a concave part for housing a semiconductor element is formed in a part of the aforementioned printed wiring substrate.

3. Manufacturing method for printed wiring substrate for semiconductor mounting described in Claim 2, characterized in that the aforementioned concave part or semiconductor mounting is formed by counterboring.

4. Manufacturing method for printed wiring substrate for semiconductor mounting described in Claim 1, characterized in that the aforementioned stacked substrate composed of organic resin material is formed so that the external dimensions, excluding the bridge parts, will be smaller than the external dimensions of the printed wiring substrate composed of organic resin material, excluding the bridge parts.

5. Manufacturing method for printed wiring substrate for semiconductor mounting described in Claim 1, characterized in that the aforementioned grooves are formed by punching.

6. Manufacturing method for printed wiring substrate for semiconductor mounting described in Claim 1, characterized in that a shaped part is furnished for part or all of the cut part for cutting the aforementioned bridge parts.

Detailed explanation of the invention

Industrial application field

This invention pertains to a manufacturing method for a printed wiring substrate for semiconductor mounting. In particular, it pertains to a manufacturing method for a packaging board which is generally called a leadless chip carrier.

In recent years, the demand to miniaturize electronic equipment and make them lighter and thinner has increased, and miniature leadless type chip components, called chip capacitors and chip resistors, that have no external leads have come to be used in the electronic components, e.g., capacitors and resistors, of that equipment. Even in semiconductor integrated circuit devices, e.g., IC and LSI, as the demand for miniaturization and higher density of the circuits has increased, the trend to make the form of the package smaller and leadless has become marked at the same time, and there has been a trend toward increasing the number of chip carriers of the miniature leadless type. These leadless chip carriers are packaged in general printed wiring boards and serve the role of IC packages.

Prior art

In the past, ceramic chip carriers have been used as miniature leadless type IC packages for semiconductor mounting. Ceramic chip carriers are fired at a high temperature after a metallized layer is formed on a green sheet and after multiple green sheets are stacked. A concave part for housing the semiconductor elements is formed approximately in the center of the aforementioned, a metal pattern is formed radially around the concave part, and said pattern is electrically connected with the pattern on the reverse side through the metallized layer on the surface of the substrate side wall. After semiconductor elements are housed in the aforementioned concave part, a package is obtained by sealing the elements with a cap made of metal or ceramic.

Chip carriers composed of organic resin material instead of the expensive ceramic chip carriers have also been proposed in (a) Japanese Kokai Patent Application No. Sho 56[1981]-2656, (b) Japanese Kokai Patent Application No. Sho 58[1983]-134450, and (c) Japanese Kokai Patent Application No. Sho 57[1982]-184240.

The aforementioned proposals have a structure where circuit patterns with through-holes are formed in printed wiring substrates that are composed of glass epoxy. After mounting the semiconductor elements, the periphery around the semiconductor elements is covered with a protective resin.

Problems to be solved by the invention

In the chip carriers according to aforementioned (a) Japanese Kokai Patent Application No Sho 56[1981]-2656 and (b) Japanese Kokai Patent Application No. Sho 58[1983]-134450, when a highly fluid resin is used as the potting resin for sealing the semiconductor elements, there is the disadvantage that the resin flows out from around the semiconductor elements to the part around the chip carrier. The metallized layer on the side wall surfaces of the chip carrier is covered, and the performance of the chip carrier decreases. Furnishing a frame to prevent the resin outflow around the semiconductor element mounting part which is on the top surface of the substrate for semiconductor mounting has been disclosed in Japanese Kokai Utility Model No. Sho 55[1980]-86342. A manufacturing method for a chip carrier with a side wall composed of plastic is also proposed by aforementioned (c) Japanese Kokai Patent Application No. Sho 57[1982]-184240. A cross section of it is shown in Figure 6. After metal patterns (8) are formed and arranged on the surface of substrate sheet (1) that uses a plastic material, lattice arm (15) made of a plastic material is adhered to the aforementioned metal pattern, and multiple leadless chip carriers are produced by cutting the center of the lattice arm using a diamond saw or other tool. (X-X') is the position of that cutting.

Cutting with a diamond saw in the aforementioned proposal requires a large amount of time, so productivity is very low, and it is difficult to provide inexpensive chip carriers.

Punching with highly productive metal dies is another tool that can also be considered. However, the disadvantage is that when the position (X-X') in Figure 6 is stamped with a metal die, the metal layer at through-hole (2) may easily separate due to the impact during punching.

According to verification experiments by the present inventors, when a printed wiring substrate, having a composition where the thickness of substrate sheet (1) was 0.5 mm and the thickness of lattice arm (15) was 0.5 mm, was stamped at position (X-X') using a metal die, separation and cracking occurred in most of the through-holes, and the conductor layer on the side wall surfaces was extremely insufficient.

The purpose of this invention is to eliminate and to remedy all of the disadvantages of the aforementioned prior art. It will provide a manufacturing method for printed wiring substrates for semiconductor mounting that is suitable for automation.

Means to solve the problems and operation

This invention will be explained in concrete terms below based on the figures.

First, Figure 1(a) and Figure 1(b) are plan views of a substrate that illustrate representative examples of the group of finished products which are arranged in the form of a lattice to become the bottom layer of the printed wiring substrates for semiconductor mounting. These printed wiring substrates are manufactured by processes (a) and (b) described in Claim 1.

Figure 2 is a plan view of a substrate on which through-holes are furnished in a lattice pattern to form the top layer and on which grooves and bridge parts have been formed. This substrate is manufactured by process (c) described in Claim 1. Then the printed wiring substrates for semiconductor mounting shown in the plan view in Figure 3 are manufactured by sticking these top layers and bottom layers together. Note that, prior to the substrate shown in Figures 1(a) and (b) by aforementioned processes (a) and (b), the substrate shown in Figure 2 can also be manufactured by process (c) described in the claim. Then, the printed wiring substrates for semiconductor mounting of this invention shown in the plan view in Figure 3 are manufactured by sticking together the substrates that become the bottom layers, shown in Figures 1(a) and (b), and the substrates that become the top layers, shown in Figure 2, the same way as the aforementioned.

Then, Figure 4 is a perspective view of the major parts of said substrate that illustrates the processes of the manufacturing method for printed wiring substrates for semiconductor mounting described in each of the claims of this invention. Figures 1(a) and (b) are front views of the printed wiring substrate sheets where, after multiple groups of conductor patterns that have through-holes are arranged and formed regularly, longitudinally and laterally on printed wiring substrate sheet (1), composed of an organic resin material, e.g., glass epoxy, glass triazine, or glass polyimide, the parts of the through-holes positioned on the external outline of the finished products in the multiple groups of conductor patterns formed on the aforementioned printed wiring substrate sheet are cut away, parts of through-holes (2) are exposed on the external side wall surfaces of the aforementioned substrates, grooves (6) are formed around the through-holes, and they [the sheets] are arranged in the form of a lattice by bridge parts (4) formed between said grooves.

Concave part (9) for housing semiconductor elements is also furnished in the center part of the aforementioned substrate by counterboring. Metal plating is applied to through-hole (2) on the external outline of the finished product and the metal pad around the concave part. Solder resist (7) is printed between said through-hole and said metal pad, and the conductor pattern is protected. Figure 2 is a stacked substrate sheet described in (e) of Claim 1. The stacked substrate sheet may be glass epoxy, glass triazine, glass polyimide, or the like. The printed wring substrate sheet with frame in the form of a lattice is formed as shown in Figure 3 when groove (6) on said stacked substrate sheet is formed to correspond to the printed wiring substrate sheet in Figure 1(a), the stacked substrate sheet in Figure 2 is matched with pilot hole (5) for affixing the metal die on the substrate sheet in Figure 1(a), and they are stuck together with an adhesive layer. When bridge parts (4) are stamped at four places with a metal die and cut, printed wiring substrates for semiconductor mounting in the form of pieces can be produced as shown in

Figure 4. In addition to the large sheet as shown in Figure 3, the substrate sheet in the form of a narrow strip as shown in Figure 5 in this case is also effective.

This invention is characterized in that, after conductor parts are formed in advance on the side wall surfaces, a frame for preventing outflow of the sealing resin is stuck on and bridge parts (4) are cut at four places. So in addition to being easy, it is difficult for cracking to occur in the substrate itself because no separation of the through-hole plating or variation in the substrate is produced, and the cut surface can be finished in an extremely satisfactorily manner.

Figure 6 illustrates a part of the manufacturing process for a conventional semiconductor device using plastic material; it shows a processing cross section when the center of lattice arm (15) is cut along (X-X'). Many metal patterns (8) arranged in the form of a square are formed on the surface of substrate sheet (1) that is composed of plastic, for example, epoxy resin with glass mixed in. Many through-holes are furnished through said substrate sheet, and one of those through-holes is indicated by symbol (2) in Figure 6. Corresponding metal pad (16) is formed on the bottom surface of this through-hole and metal pattern (8) and metal pad (16) are electrically connected. Lattice arm (15), which is the same material as substrate sheet (1), is adhered, and this lattice arm (15) is positioned to give a side wall on the line on which through-holes (2) are arranged. Through-holes (2) appearing on the top surface of substrate (1) are left. Integrated circuit chip (13) is adhered to the center of this lattice arm (15) with an epoxy adhesive layer and is connected to metal pattern (8) by wire bonding (14).

Figures 7(a) and (b) are perspective views of the printed wiring substrate for semiconductor mounting described in Claim 4 of this invention. It is characterized in that groove (6) of the stacked substrate sheet is stamped larger than the groove in the printed wiring substrate, and for this reason, the external dimensions of the aforementioned stacked substrate sheet, excluding bridge parts (4), will be smaller than the aforementioned substrate. After this substrate is packaged in a general printed wiring board, this substrate has the advantage that it is easy to see whether or not solder has overflowed into the through-holes in the side wall surfaces or whether bridges have occurred in the adjacent through-holes. In this case, too, when aforementioned stacked substrate sheet (10) and substrate sheet (1) are stuck together, they are aligned by pilot hole (5) and bridge parts (4) are stamped with a metal die to separate them into pieces. When these bridge parts (4) are stamped, attaching shaped part (18) to a part of the cut part of said bridge parts described in Claim 6 serves the purpose of positioning during mounting in a general printed circuit board. By attaching a shaped part to all of the cut parts of the bridge parts, cracking from the corner parts of the package and peeling of the solder resist can be reduced and a beautiful package from a design standpoint can be obtained.

Figure 8 shows a cross section where integrated circuit chip (13) has been mounted in concave part (9) on printed wiring substrate (15) for semiconductor mounting that has been

stamped according to each of the claims of this invention. Said integrated circuit chip (13) and metal pattern (8) have been connected by wire bonding (14), electronic component cap (21) has been mounted after resin (20) is injected from a dispenser or the like, and resin sealing has been performed by heating.

Effects of the invention

As stated above, this invention has the advantages that the economic cost is lower than conventional packages using ceramic as the material, the form of the package can easily be smaller and thinner, and connections will not be damaged even when packaged in general printed wiring boards. A multi-layer structure is also possible with packages that use the same plastic material, and by providing the cutting method of this invention, there is also the advantage that the cut surfaces can be finished easily and rapidly, and furthermore, extremely satisfactorily.

Brief explanation of the figures

Figures 1(a) and (b) and Figures 2-4 are front views and a perspective view of the major parts of a substrate used for the manufacturing process for a printed wiring substrate for the semiconductor mounting described in each of the claims of this invention. Figure 5 is a front view of the aforementioned substrate sheet which shows that it is also effective when the size of the substrate sheet of this invention is a narrow strip. Figure 6 is a cross section that shows, among the manufacturing processes for the printed wiring substrate using conventional plastic as the material, the cutting position (X-X') to separate each of the printed wiring substrates into pieces. Figures 7(a) and (b) are a front view and perspective view of the printed wiring substrate described in Claim 4. Figure 8 shows a cross section of the final structure where an integrated circuit chip is packaged by wire bonding and resin sealed in the concave part on a printed wiring substrate for semiconductor mounting that has been stamped according to each of the claims of this invention.

1 Printed wiring substrate sheet
2 Through-hole
3 Part of the substrate
4 Bridge part
5 Pilot hole
6 Groove
7 Solder resist
8 Metal pattern
9 Concave part for semiconductor mounting
10 Stacked substrate sheet

11 Frame for sealing
12 Substrate sheet in the form of a narrow strip
13 Integrated circuit
14 Bonding wire
15 Lattice arm
16 Metal pad
17 Sealing frame with smaller dimensions than the printed wiring substrate
18 Shaped part
19 Printed wiring substrate for semiconductor mounting
20 Sealing resin
21 Electronic component cap

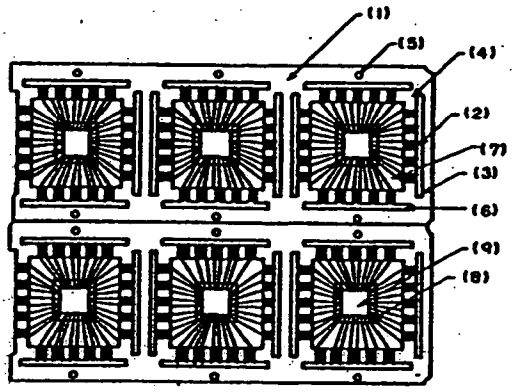

Figure 1(a)

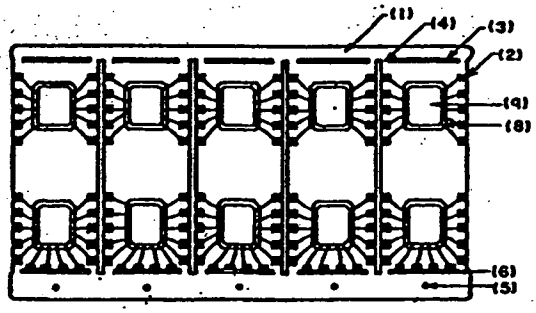

Figure 1(b)

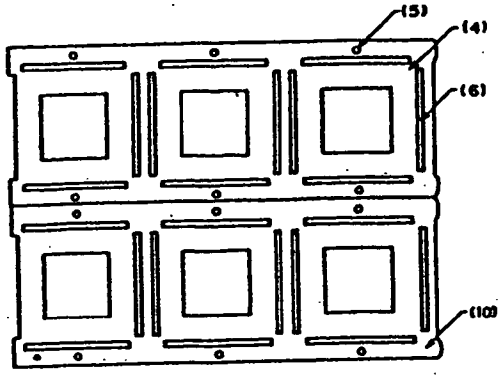

Figure 2

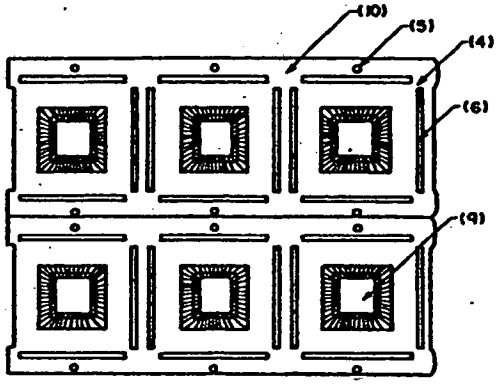

Figure 3

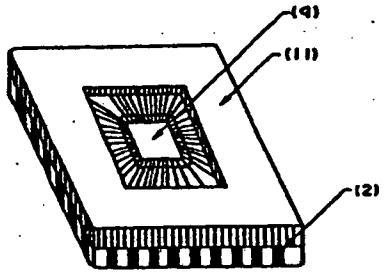

Figure 4

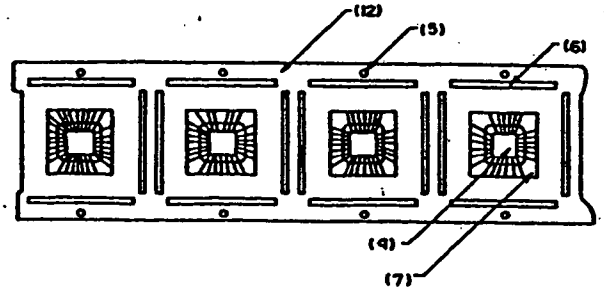

Figure 5

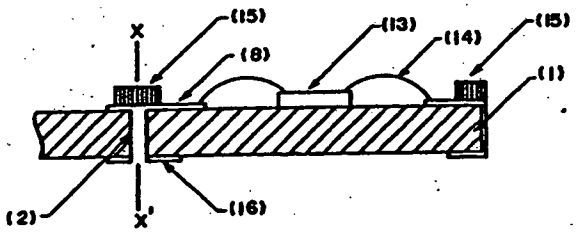

Figure 6

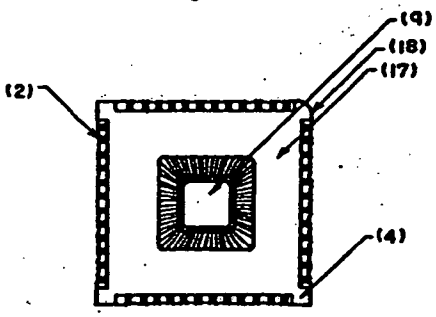

Figure 7(a)

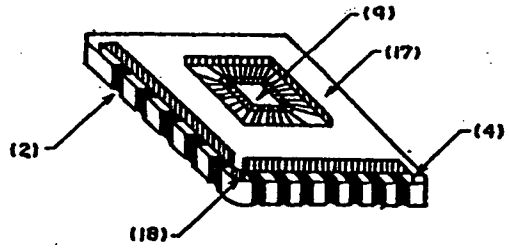

Figure 7(b)

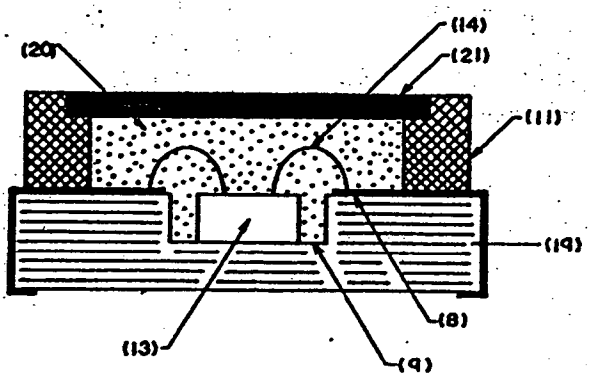

Figure 8